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Synchronous rectifier in DC/DC converters

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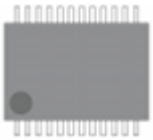

This paper is presented design of synchronous rectifiers for forward DC/DC converter of the switch-mode power supplies. Firstly are introduced different circuit diagrams of these rectifiers. Than are theoretically determined the limits of efficiency improvements that can be obtained by synchronous rectifiers. Finally are compared conversion efficiencies of control-driven SRs with those of different self-driven SR implementations. Specifically, performance comparisons of the forward converters with RCD-clamp and active-clamp reset are made.

Introduction

The conduction losses of diode rectifier contribute significantly to the overall power losses in a power supply, especially in low output-voltage applications [1]. The rectifier conduction losses are proportional to the product of its forward-voltage drop, V_F, and the forward conduction current, I_F.

Synchronous rectification (SR) is used in DC/DC converters when low output voltage is less than 5V and high current is needed [2]. Synchronous rectification utilizes power MOSFETs to rectify the output voltage of the power transformer. These MOSFETs are synchronized to the converter frequency and perform more efficiently the rectification of the output voltage than rectifying diodes due to the low I.R drop through the channel. The N channel power MOSFET offers the lowest ON resistance and is relatively inexpensive [4].

On the other hand, operating in the MOSFET III quadrant, a synchronous rectifier presents a resistive V-I characteristic, as shown in Fig. 1. Under certain current level, the forward-voltage drop of a synchronous rectifier can be lower than that of a diode rectifier, and consequently reduces the rectifier conduction losses. Due to the fact that synchronous rectifiers are active devices, the design and utilization of synchronous rectification need to be properly made.

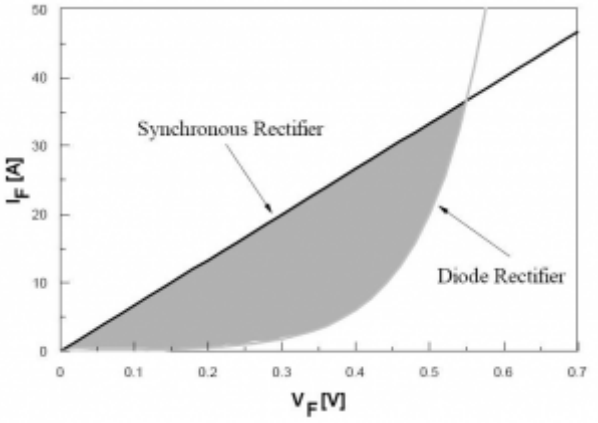

Fig. 1 Comparison of the forward voltage between diode rectifier and synchronous rectifier (gray area has conduction losses saving by using synchronous rectifiers)

Synchronous rectification in forward converter

A low-voltage plus high-current DC power supply is urgently required in the next-generation computer and communications equipment. The first idea is to use a forward converter, refer to Fig. 2, which can perform low-voltage plus high-current output voltage [1],[5]. The two diodes D_1 and D_2 can be normal rectifier diodes, rectifier Schottky diodes, or MOSFET transistors. Fig. 3 shows the efficiency gain of the following three types of forward converters needed to construct a low-voltage high-current power supply:

- Forward converter using traditional diodes
- Forward converter using Schottky diodes
- Synchronous rectifier using low forward-resistance MOSFET

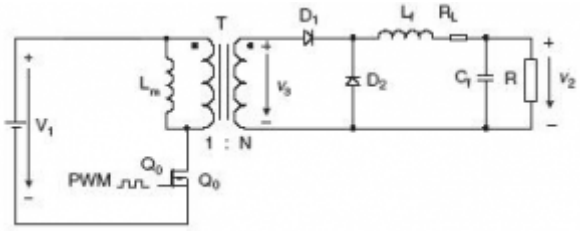

Fig. 2 Forward converter using traditional diodes

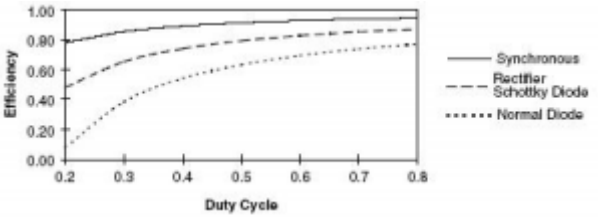

Fig. 3 Efficiencies of different types of forward converter

As the operating voltages increase, the design of rectifiers requires more attention because the devices forward-voltage drop constitutes an increasing fraction of the output voltage. The forward-voltage drop across a switch-mode rectifier is in series with the output voltage, so losses in this rectifier will almost entirely determine its efficiency. The synchronous rectifier circuit has been designed primarily to reduce these losses.

Circuit configurations

Based on the method employed in driving SRs, all of them can be classified into two groups: control-driven and self-driven. In a control-driven SR implementation, the SRs are driven by gate-drive signals derived from the gate-drive of the main switch. In a self-driven SR implementation, the SRs are driven directly with the secondary voltage of the transformer. As a result, the self-driven SR approach is very attractive since it is simple and requires a minimum number of components. However, the performance of self-driven SRs depends on the resetting method of the power transformer since the freewheeling synchronous rectifier is driven by the reset voltage. Ideally, it would be desirable that the resetting time be equal to the off-time of the primary switch. Then the output current would freewheel through the SR for the entire off (freewheeling) time.

Forward Converter with RCD-Clamp and Self-Driven SRs

The forward converter with self-driven SRs and its key waveforms are shown in Fig. 4 [3]. In this circuit, synchronous rectifiers SR_3 (Q_3 and D_3) and SR_4 (Q_4 and D_4) are crosscoupled to the secondary winding of the transformer and are directly driven by the secondary voltage. Since no driver or control circuit is used to provide the gate-drive signals, this implementation of synchronous rectification is the simplest possible. However, its performance is strongly dependent on the method of the transformer core resetting, because the gate-drive signal for synchronous rectifier SR_4 is derived from the reset voltage.

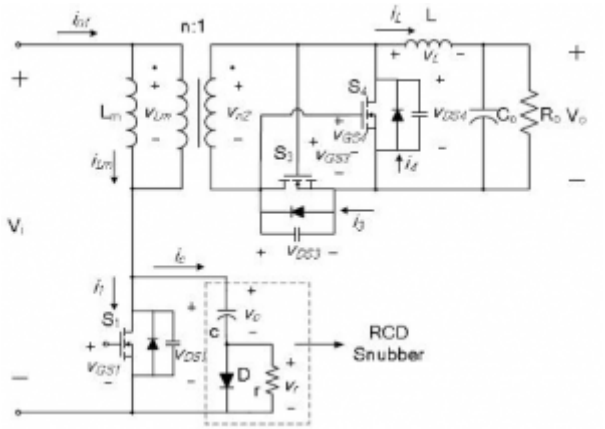

Fig. 4 Forward converter with RCD-clamp and self-driven SRs

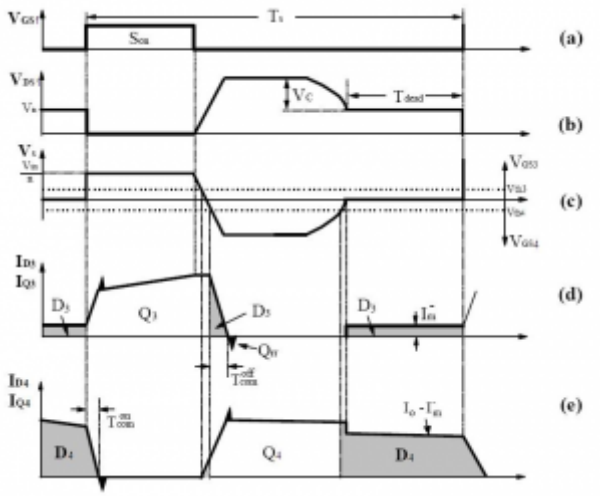

Fig. 5 Waveforms of a forward converter with RCD clamp and self-driven SRs: a) gate-drive signal, b) drain-to-source voltage of primary switch, c) secondary winding voltage, d) current through SR_3 and e) current through SR_4

As can be seen from the waveform in Fig. 5d, once the transformer reset is completed, the magnetizing current of the transformer, I_m-, starts flowing through the body diode of SR_2. The magnitude of this current is given by:

$$I_m^- = N\frac{V_C}{\sqrt{L_m/C_S}} \tag{1}$$

where N is the turns ratio of the transformer, V_C is the transformer reset voltage, Lm is magnetizing inductance of the transformer, and C_S is the total capacitance seen at the drain of the primary switch.

Also, as can be seen from the waveforms in Fig. 5e, after the transformer reset is completed, the difference between load current I_0 and magnetizing current I_m- is diverted from transistor Q_4 to the body diode, D_4, of SR_4. Due to relatively high forward-voltage drops of the body diodes of SR_3 and SR_4, the efficiency of synchronous rectification is reduced. The efficiency losses due to the body-diode conduction depend on the duration of the dead time, T_{dead}, and the forward-voltage drops of the body diodes, V_{BD}. These losses can be minimized by connecting Schottky diodes in parallel with SR_3 and/or SR_4 or by minimizing the conduction times of D_3 and D_4.

Forward Converter with Active Clamp and Self-Driven SRs

The forward converter with active-clamp reset and its key waveforms are shown in Fig. 6 [3]. As can be seen, the active-clamp-reset approach minimizes the duration of the dead time since the transformer core is reset during almost the entire off time of the primary switch. As a result, the conduction time of transistor Q_4 is maximized, the time during which D_3 is conducting magnetizing current is minimized. Consequently, the conversion efficiency of the converter with the active-clamp reset is improved relative to the RCD-clamp counterpart.

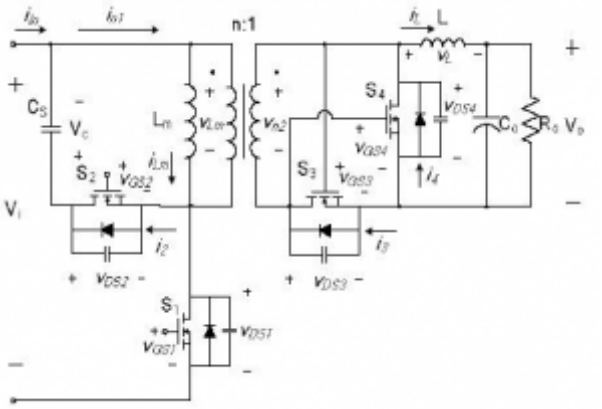

Fig. 6 Forward converter with active-clamp and self-driven SRs

Also, the active-clamp reset approach minimizes voltage stress on the primary switch. However, the active clamp approach requires an extra switch and its associated gate drive, compared to the same circuit with the RCD-clamp reset. From this perspective, it is much simpler and more economical to use a Schottky diode in parallel with SR_3 to improve the efficiency of the RCD-clamp circuit than it is to implement the active clamp. Therefore, the active-clamp approach is a viable choice in synchronous-rectifier applications where voltage stress and soft-switching are important design considerations.

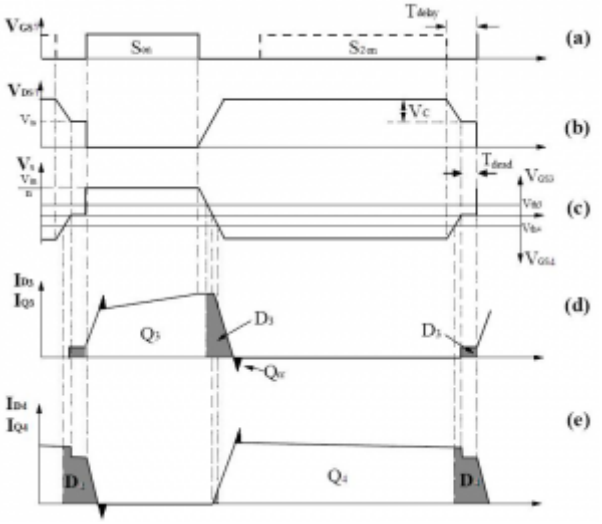

Fig. 7 Waveforms of a forward converter with active-clamp and self-driven SRs: a) gate-drive signals, b) drain-to-source voltage of primary switch, c) secondary winding voltage, d) current through SR_3 and e) current through SR_4

Forward Converter with RCD Clamp and Control-Driven SRs

The forward converter with control-driven SRs and its key waveforms are shown in Fig. 8 [3]. In this circuit, transistors Q_3 and Q_4 are driven by gate-drive signals derived from the primary-switch gate drive. As a result, the conduction times of the synchronous rectifiers are independent of the transformer-resetting method, but solely depend on the timing of the gate-drive signals. However, as can be seen from Figs. 9d and 9e, while driving the SRs from the control circuit results in the maximum conduction time of Q_4, it has no effect on the conduction time of the magnetizing current though diode D_3 during the dead time. Namely, since during the dead time transistor Q_3 is off (gate-drive to Q_3 is low), the conduction of diode D_3 during the dead

time with control-driven SRs (see Fig. 8) is exactly the same as for the self-driven SRs (see Fig. 4).

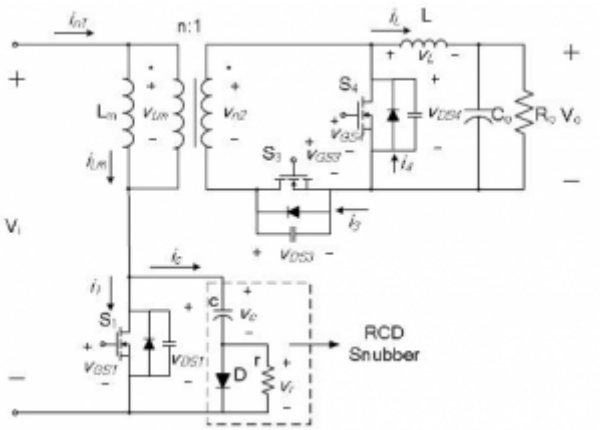

Fig. 8 Forward converter with RCD-clamp and control-driven SRs

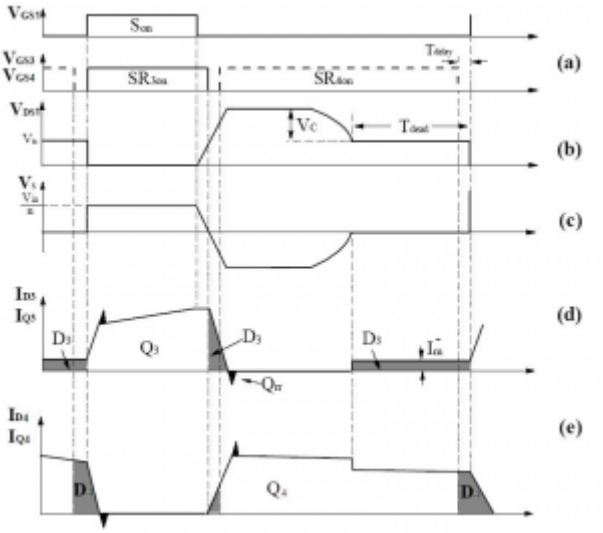

Fig. 9 Waveforms of a forward converter with RCD clamp and control-driven SRs: a) gate-drive signal, b) drain-to-source voltage of primary switch, c) secondary winding voltage, d) current through SR_3 and e) current through SR_4

Forward Converter with Active Clamp and Control-Driven SRs

The basic circuit configuration shown in Fig. 10 is similar to that shown in Fig. 6. The only difference is that the whole circuit in Fig. 10 is fully-controlled by the microcontroller.

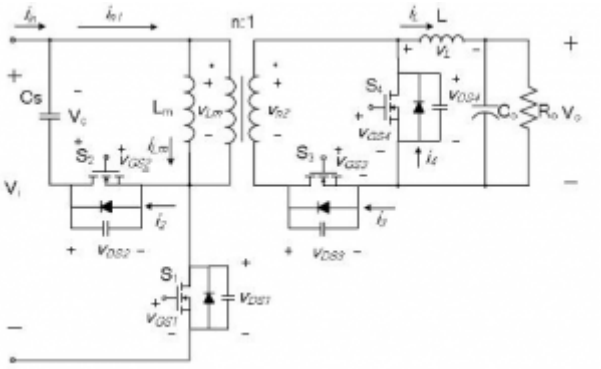

Fig. 10 Forward converter with active-clamp and control-driven SRs

In practical applications, this ideally complementary drive is not possible. The driving pulses are shown in Fig. 11. The dead times are included that will not occur brief overlapping of the gate-drive signals simultaneously that would short on the primary or the secondary, causing an increased primary or secondary current, and thus would lower efficiency or, in severe cases, would cause converter failure.

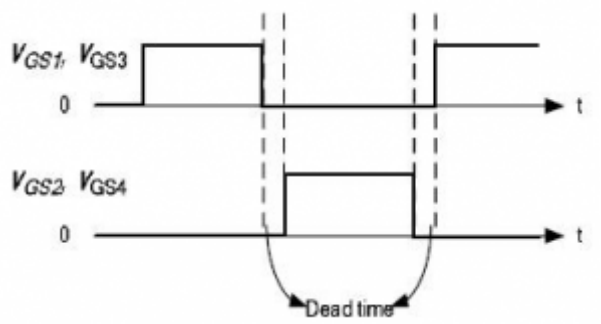

Fig. 11 Waveforms of driving pulses for forward converter with active-clamp and control-driven SRs

Efficiency limits of synchronous rectification

The efficiency improvement that can be achieved by replacing Schottky rectifiers with SRs is a complex function of many parameters. The most important are the output voltage, output current, SR on-resistance, forward-voltage drop of Schottkies that are being replaced by SRs, the transformer resetting method, efficiency of the converter with Schottkies, and implementation of SRs (i.e., with or without Schottkies in parallel with SRs). Generally, the efficiency of a converter can be expressed as

$$\eta = \frac{P_0}{P_0 + P_{loss} + P_{REC}} \tag{2}$$

where P_0 is the output power, P_{loss} are the total losses excluding the rectifier losses, and P_{REC} are the rectifier losses. For a converter with Schottky rectifiers, the efficiency is

$$\eta_{SH} = \frac{P_0}{P_0 + P_{loss} + P_{SH}} \tag{3}$$

Similarly, for the same converter with SRs, the efficiency is

$$\eta_{SR} = \frac{P_0}{P_0 + P_{loss} + P_{SR}} \tag{4}$$

Eliminating P_{loss} from the above equations, the efficiency of the converter with SRs, η_{SR}, can be expressed as a function of the efficiency of the converter with the Schottkies, η_{SH},

$$\eta_{SR} = \frac{P_0}{P_0/\eta_{SH} + P_{SH} + P_{SR}} \tag{5}$$

The power losses in the Schottky rectifiers can be calculated as

$$P_{SH} = V_{SH}.I_0 \tag{6}$$

where V_{SH} is the forward-voltage drop of the Schottkies, and I_0 is the output current. The power losses of the self-driven SRs, P_{SR}^{sd}, for both RCD-and active-clamp reset are given by:

$$P_{SH}^{sd} = R_{DS(on)} I_0^2 (1 - D_{dead}) + V_D I_0 D_{dead} + P_{gate} + P_{PREC} \tag{7}$$

where $R_{DS(on)}$ is the on-resistance of SRs, $D_{dead} = T_{dead}/T_s$ is the dead-time duty cycle, V_D is the forward-voltage drop of the antiparallel diodes across SR_3 and SR_4, P_{gate} are the gate-driven losses, and P_{RREC} are the power losses associated with the reverse-recovery of the body diodes of the SRs. It should be noted that Eq. 7 is derived assuming that commutation times T_{com} on and T_{com}^{off} are zero, that synchronous rectifiers SR_3 and SR_4 have identical on resistance ($R_{DS(on)3} = R_{DS(on)4} = R_{DS(on)}$), and that diodes D_3 and D_4 have identical voltage drops ($V_{D3} = V_{D4} = V_D$) which are independent of their currents.

For self-driven SRs with active-clamp reset, the dead time is very short relative to a switching period, and therefore, $D_{dead} >> 0$. However, for the converter with the self-driven SRs and with the RCD-clamp reset, this duty cycle usually cannot be neglected. In this case, the losses depend on the duration of the dead time and V_D of the antiparallel diodes of the SRs. Generally, these diodes can be the body diodes of SRs ($V_D = V_{BD}$) or externally added Schottkies in parallel with SRs ($V_D = V_{SH}$). The power loss of the control-driven SRs is given by:

$$\begin{aligned} P_{SR}^{cd} = {} & R_{DS(on)} I_0^2 (1 - D_{dead}) + R_{DS(on)} (I_0 - I_m^-)^2 (D_{dead} - D_{delay}) \\ & + V_D I_m^- D_{dead} + V_D (I_0 - I_m^-) D_{delay} + P_{gate} + P_{PREC} \end{aligned} \tag{8}$$

where $D_{delay} = T_{delay}/T_s$ is the delay-time duty cycle, and T_{delay} is the delay time between the SR_4 gate-drive turn-off and SR_3 gate-drive turn-on as indicated in Fig. 6b. The gate-drive losses, P_{gate}, are a function of the gate-to-source voltage of SR, frequency, and gate charge required to charge SRs' capacitance to the gate-source voltage. A method of estimating these losses for self-driven SRs was presented in [5]. For control-driven SRs these losses are higher since it includes also the losses in the external drivers and their associated logic.

The reverse-recovery losses, P_{RREC}, are only presented in implementations where the body diode of the SR is conduction (no Schottky in parallel with SR). When the gate-drive losses and the reverse-recovery losses are neglected ($P_{gate} = P_{RREC} <$

$$\frac{1}{\eta_{SR}^{sd}} = \frac{1}{\eta_{SH}} - \frac{V_{SH}}{V_0} \left[1 - \frac{R_{DS(on)} I_0}{V_{SH}} (1 - D_{dead}) - \frac{V_D}{V_{SH}} D_{dead} \right] \tag{9}$$

Since for the forward converter with self-driven SRs and active-clamp reset (Ddead <

$$\frac{1}{\eta_{SR}^{acl}} = \frac{1}{\eta_{SH}} - \frac{V_{SH}}{V_0} \left[1 - \frac{R_{DS(on)} I_0}{V_{SH}} \right] \tag{10}$$

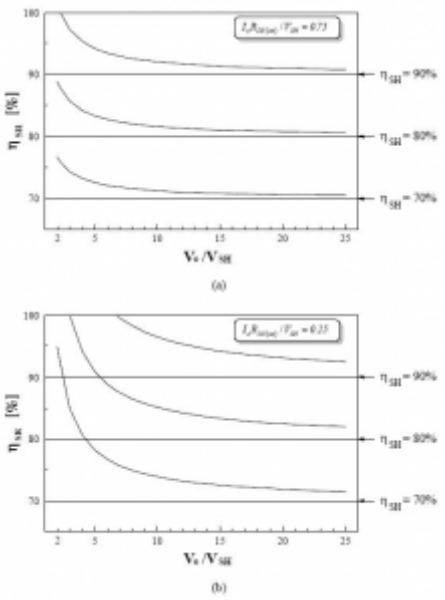

Fig. 12 Efficiency limits of forward converter with self-driven SRs and active-clamp reset and control-driven SRs with small gate-drive timing delay (D_{delay} >> 0) and magnetizing current I_m^- <0: a) α = $R_{DS(on)}$·I_0/V_{SH} = 0,75, and b) α = 0,25

Eqs. 9 and 10 can be regarded as the best-case efficiency limits of different SR implementations. The efficiencies of the forward converter with control-driven SRs, η_{SR}^{cd}, is given by:

$$\begin{aligned}\frac{1}{\eta_{SR}^{cd}} = \frac{1}{\eta_{SH}} - \frac{V_{SH}}{V_0}\Big[1 - \frac{R_{DS(on)}I_0}{V_{SH}}(1 - D_{dead}) \\ - \frac{R_{DS(on)}I_0}{V_{SH}}\left(1 - \frac{I_m^-}{I_0}\right)^2 (D_{dead} - D_{delay}) \\ - \frac{V_D I_m^-}{V_{SH} I_0} D_{dead} - \frac{V_D}{V_{SH}}\left(1 - \frac{I_m^-}{I_0}\right) D_{delay}\Big]\end{aligned} \tag{11}$$

If magnetizing current I_m^- <0 so that its losses can be neglected, and if the delay time is short so that D_{delay} >> 0, Eq. 11 simplifies to Eq. 10. Fig. 12 shows the plots of this equation. These plots present the efficiency of a converter with SRs, η_{SR} as a function of the normalized output voltage, V_0/V_{SH}. The efficiency of the converter with Schottky rectifiers, η_{SH}, and $\alpha = I_0 \cdot R_{DS(on)}/V_{SH}$ are the parameters. Parameter α represents the ratio of the forward-voltage drop of the SR at output current, I_0, to the forward-voltage drop of the Schottky.

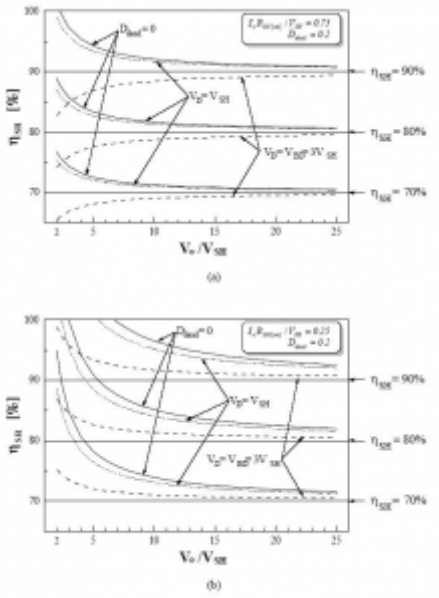

Fig. 13 Efficiency limits of forward converter with self-driven SRs and RCD-clamp reset for D_{dead} = 0,2: a) α = $R_{DS(on)}$·I_0/V_{SH} = 0,75, and b) α = 0,25

As can be seen, the efficiency improvement for a given α and a given V_{SH} is lower at higher output voltages, V_0. Also, for the same output voltage, the efficiency gain achieved by synchronous rectification is higher for converters with higher efficiencies with Schottky diodes, η_{SH}. Similarly, the efficiency improvement is larger for smaller α, i.e., for better SRs (smaller on-resistance) or lower output currents. Fig. 13 shows the plots of Eq. 9 for D_{dead} = 0,2 for the SR implementation with a Schottky in parallel with SR_4 ($V_D = V_{SH}$) and without a Schottky ($V_D = V_{BD} = 3V_{SH}$). Also, for reference, the curves for D_{dead} = 0 (see Fig. 12) are shown. The efficiency of the converter with the RCD-clamp reset is strongly dependent on the SR implementation. For the implementation with Schottky diodes, the efficiency improvement is slightly lower than that of the control-driven SRs or self-driven SRs with an active-clamp reset. However, when the body diode of SR_4 is used to free-wheel the output current, the difference is very significant. In fact, under certain conditions the efficiency of synchronous rectification can be lower than that of Schottky diodes, as illustrated in Fig. 13a for $V_D = V_{BD} = 3V_{SH}$.

Conclusion

In this paper was presented design of synchronous rectifiers for forward DC/DC converter. There were introduced control-driven and self-driven circuit diagrams of these rectifiers. The limits of efficiency improvements that can be obtained by synchronous rectifiers are primarily a function of the output voltage, output current, on-resistance of the SR, and the forward-voltage drop of Schottky rectifiers replaced by SRs. In the end, performance comparisons of the forward converters with RCD-clamp and active-clamp reset were made.

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